



ETSystemMemory™

OVERVIEW

LogicVision's ETSystemMemory provides a complete solution for the at-speed testing and diagnosis of component memories. The solution provides support for most SRAM and DRAM memories, including those that utilize burst modes of operations such as DDR and QDR memories. ETSystemMemory, with its run-time programmable algorithms, provides the flexibility for users to customize the execution of the memory test without relying on the ASIC designer to hard code all of the possible combinations of algorithms into the controller. This greatly reduces the risk that functional memory tests will have to be developed as a result of discovering new defect types not screened with standard test algorithms.

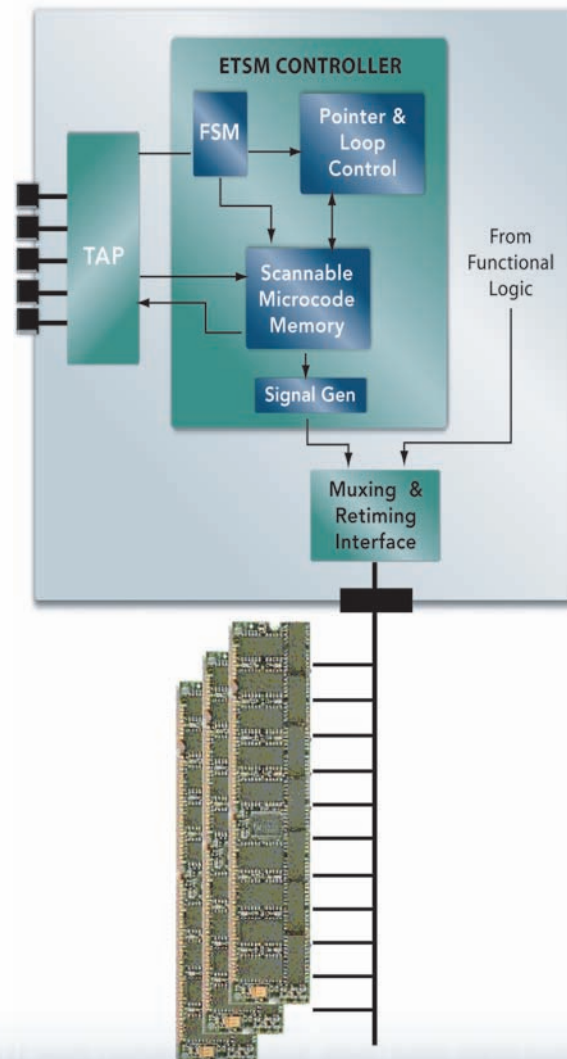
In addition to the programmable algorithms, ETSystemMemory accesses and tests the memories at application speed. This allows the memory subsystem to be tested for noise, timing marginality, and power distribution problems. These defects cannot be detected using boundary scan test techniques. Using the LogicVision TAP, the ETSystemMemory controller can be accessed using the IEEE 1149.1 protocol. An automated design kit expedites the generation, integration and verification of the ETSystemMemory controller and interface IP as well as the IEEE 1149.1 TAP into an ASIC or SOC design at either the RT or netlist levels.

BENEFITS

- Reduced board manufacturing costs:
 - › Simplified 1149.1 interface means cheaper fixtures
 - › Higher throughput: test times much faster than in-circuit
 - › Lower escape rates from higher fault coverage
 - › Improved debug capability on new boards
- Reduced system and field service costs:
 - › Lower escapes from manufacturing
 - › Re-use of self test improves accuracy of diagnosis and efficiency of repair process
 - › Simpler and cheaper field-service testers

CAPABILITIES

- At-Speed testing of external SRAM, DRAM
- At-Speed testing of memory buses
- Supports an unlimited number of memories, ports and configurations
- Run-time programmable memory test algorithms
- Run-time programmable waveforms
- Diagnostic data for FRU identification or full failure bit-map
- Comprehensive automation for IP integration and verification as well as test pattern generation



High Level Architecture

RTL Integration and Automation

ETSystemMemory is a complete test solution that includes RTL design objects for the external memory test controller and controller interface logic and a fully automated integration flow. As a front-end RTL solution, ETSystemMemory takes in appropriate design related information about the target memory cluster and various test requirements. Based on this information, it automatically generates:

- Embedded test controller design objects in synthesizable Verilog RTL
- Controller interface logic design objects in synthesizable Verilog RTL
- A Verilog test bench to verify the functionality of the embedded test structures in simulation
- Synthesis scripts targeting a single ASIC

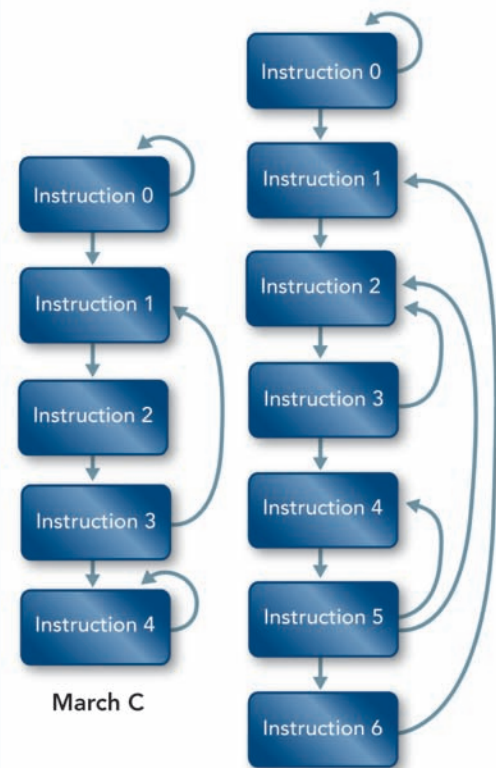
Programmable User Defined Test Algorithms

An innovative microcode memory architecture supports the programming of virtually any memory test algorithm. The algorithms may be hard coded at design time or shifted in at run-time. Supported memory test algorithms include popular $O(N)$, $O(N \log N)$ and $O(N^2)$ algorithms such as March C, Moving Inversions, Galpat, GalRow, GalCol, Walking Ones/Zeros, Butterfly, and Bit Surround Disturb. Most algorithms require less than 8 instructions or about 300 bits of memory implemented as synthesizable registers. A large library of algorithms is also provided to use directly or as a reference for user customized algorithm development.

Diagnostics

ETSystemMemory supports two forms of diagnostics. A *Result Array* is used for the identification of Field

Replaceable Units (FRUs). Each bit within this array is mapped to a predetermined FRU through address and data mapping. At the end of the test, individual bit values within the Result Array directly identify faulty FRUs. A *Stop-On-Error* approach is also supported to provide detailed diagnosis down to the memory bit level or memory bus line. In this approach, the embedded test controller stops on mis-compare and fail data is then scanned out serially. The embedded test controller then restarts/resumes testing to stop on the next error.



March C

Bit Surround Disturb

Efficient Algorithm Programming

ABOUT LOGICVISION

LogicVision, Inc. (NASDAQ: LGVN), provides unique yield learning capabilities in the design for manufacturing space. These capabilities enable its customers, leading semiconductor companies, to more quickly and efficiently learn to improve product yields. The company's advanced Design for Test (DFT) product line, ETCreat, works together with ETAccess and SiVision yield learning applications to enable increased profit by reducing device field returns, reducing test costs,

and accelerating both time to market and time to yield. LogicVision solutions are used in the development of semiconductor ICs for products ranging from digital consumer goods to wireless communications devices and satellite systems. LogicVision was founded in 1992 and is headquartered in San Jose, California. For more information visit www.logicvision.com

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