LogicVision

THE YIELD LEARNING COMPANY

# ET*Compression*™

## OVERVIEW

ET*Compression* is a deterministic test compression solution that builds upon LogicVision's industry leading embedded logic test solutions. In addition to providing test time and test volume compression values equal to other 3rd party compression solutions, ET*Compression* uniquely provides true at-speed launch-on-shift test application using LogicVision's patent-pending *Burst-Mode*™ test timing architecture. This provides both very high transition fault coverage as well as signal integrity screening through run-time control of internal scan rates and functional clock cycle spreading. A hierarchical architecture provides both high scalability and full core reuse leading to significant integration efficiencies and time-to-market savings.

The automated RT level test analysis, generation and insertion flow ensures low impact to the design schedule. Full and tight integration to all major 3rd party physical design flows ensures no impact to design performance.

## BENEFITS

- Over 10x test time and 100x test volume reduction
- Reduced Test Cost:
  - Short test times
  - Minimal tester hardware requirements
- Reduced Field Returns:
  - High transition fault coverage
  - Signal integrity screening
- Shortened Time-To-Market:
  - Quick DFT integration
  - No impact on timing closure
  - No impact on physical design flow
  - Fully re-usable embedded test inserted cores

## CAPABILITIES

- Patented *Burst-Mode*™ test timing architecture for true at-speed test application and power control
- Comprehensive RTL automation flow for fast test integration
- IEEE 1500 compliant distributed test access architecture and patented core Shared Isolation for hierarchical test integration
- On-chip run-time programmable masking for X-state handling

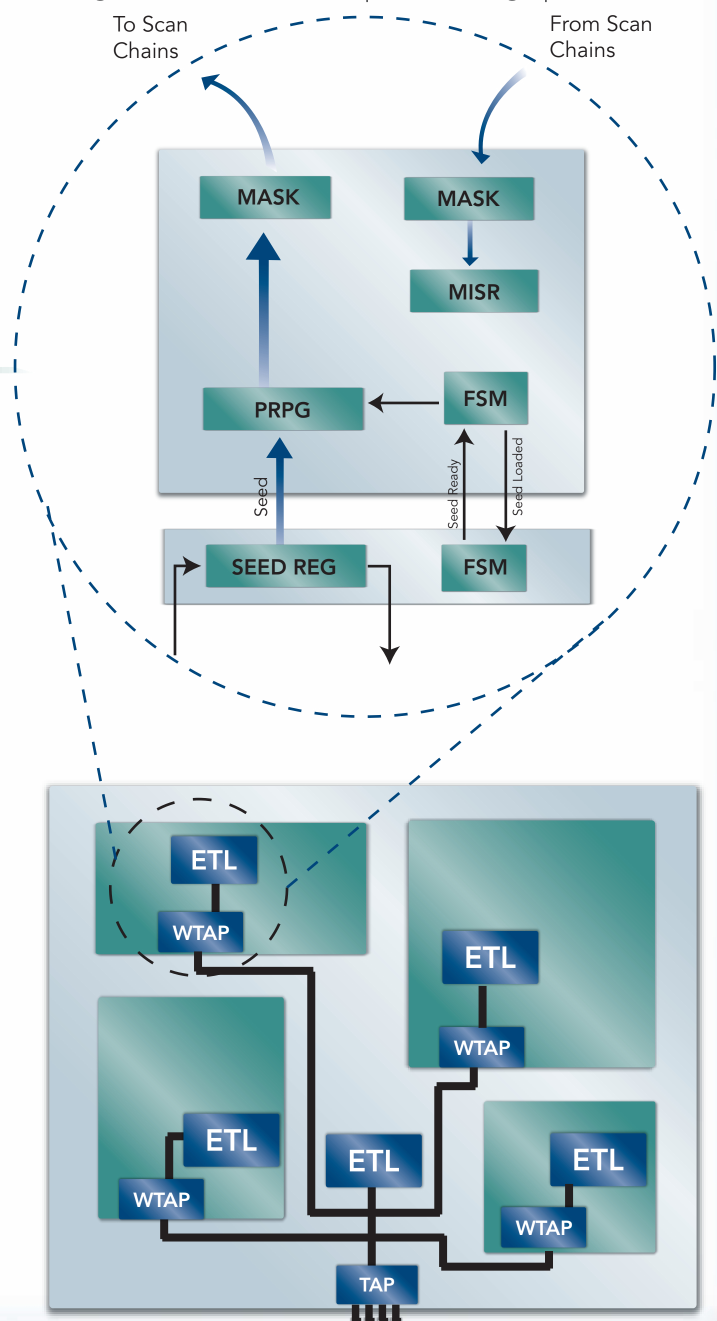


Figure 1: ET*Compression* Architecture

# ET*Compression*™

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## PRODUCT DESCRIPTION

ET*Compression* builds upon LogicVision's field proven ET*Logic* technology. Figure 1 shows the ET*Compression* architecture. A Pseudo-Random Pattern Generator (PRPG) drives the scan chains and a Multiple-Input Signature Register (MISR) compresses the scan chain output values into a signature. A run-time programmable X-masking circuit is used to mask unknown (X) values that would corrupt the MISR signature. The input mask is used to load constant values in scan chains with hold time problems. This reduces the number of X values propagating to other scan chains. Compressed patterns (or seeds) are shifted at low speed, typically 10-50 MHz, from the tester to a shadow register in the Test Access Port (TAP) or Wrapper TAP (WTAP) of an embedded block (or core). The TAP and WTAP are implemented according to the IEEE 1149.1 and IEEE 1500 standards respectively. While each seed is being shifted in, the current test pattern is decompressed by the PRPG and loaded into the scan chains at a frequency which is runtime programmable and which is often higher than the tester speed. This makes the PRPG reseeding approach attractive because it does not require shifting test data in and out of the scan chains at the frequency imposed by the tester interface. Using a faster frequency to load scan chains increases throughput and/or allows the circuit to operate at a power level that is representative of the functional mode, which has been shown to be very useful in the characterization of power grids.

The clocking approach used contributes significantly to the level of test compression achievable. First, a launch-on-shift (or skewed-load) approach is used which has been shown to require up to an order of magnitude fewer patterns to achieve the same transition fault coverage than when the launch-on-capture (or double-capture) approach is used. The scan enable signal is pipelined locally to each domain to facilitate timing closure.

Second, all multiple-cycle paths and cross-domain logic are tested concurrently so that there is no need to rerun patterns with different clock edge placement and masking configurations. This is done in a way so that both fault simulation and test generation are purely combinational to minimize run time.

During the capture phase, all functional clocks are enabled to produce a burst of clock cycles. The burst is long enough to make sure that the supply has time to stabilize before the launch and capture cycles. For each clock domain, the clock burst is configurable at runtime to mimic the functional mode of operation from a timing and power point of view. This is essential to catch subtle problems related to crosstalk or IR drop, for example.

The alignment of synchronous clock domains is preserved.

In order to further improve test compression efficiency, ET*Compression* supports test point insertion. Test points are inserted in a non-optimized, gate-level representation of the circuit. Layout tools are now capable of restructuring the logic and eliminating any timing impact.

LogicVision's advanced LV2005TM RTL automation flow. This fully hierarchical flow ensures limited impact to the design schedule. The LV2005 flow is also tightly integrated to all major 3rd party physical design flows, including RTL-to-GDSII, and has no impact to design performance.

ET*Compression* can be used as a stand-alone test strategy or in conjunction with LogicVision's random pattern based ET*Logic*™ products. Both approaches use a common embedded architecture, requiring no additional design effort to take advantage of the unique benefits offered by each.

## ABOUT LOGICVISION

LogicVision, Inc. (NASDAQ: LGVN), provides unique yield learning capabilities in the design for manufacturing space. These capabilities enable its customers, leading semiconductor companies, to more quickly and efficiently learn to improve product yields. The company's advanced Design for Test (DFT) product line, ET*Create*, works together with ET*Access* and SiVision yield learning applications to enable increased profit by reducing device field returns, reducing test costs, and accelerating both time to market and time to yield. LogicVision solutions are used in the development of semiconductor ICs for products ranging from digital consumer goods to wireless communications devices and satellite systems. LogicVision was founded in 1992 and is headquartered in San Jose, California. For more information visit www.logicvision.com.


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