LogicVision

THE TEST AND YIELD LEARNING COMPANY

ET*Boundary*™

OVERVIEW

LogicVision's ET*Boundary* provides a complete solution for the creation and integration of boundary scan cells and related control logic for embedded test and diagnosis of integrated circuit (IC) semiconductor I/O as well as test and diagnosis of board-level interconnect nets between ICs. Access to the boundary scan cells is provided through LogicVision's Test Access Port (TAP) interface using the IEEE 1149.1 (JTAG) and IEEE 1149.6 (ACJTAG) protocols. ET*Boundary*'s highly automated integration flow reduces IC engineering development effort and improves time-to-market.

ET*Boundary* supports standard 1149.1 boundary scan cells, 1149.1 custom boundary scan cells, and 1149.6 boundary scan cells for differential I/O cells driving AC-coupled nets. It also provides a unique 1149.1-based solution for contactless testing of I/O using boundary scan. In all cases, the boundary scan logic can be accessed throughout the life of the IC, including manufacturing test, silicon debug, and system verification. The result is that both I/O cell defects and inter-IC board interconnect problems are detected prior to shipment, reducing field support costs and increasing customer satisfaction.

CAPABILITY	DESCRIPTION	KEY BENEFITS
IEEE 1149.1 Standard Boundary Scan	Generates and integrates RTL code for customizable 1149.1-compliant TAP controller and boundary scan cells. Provides library of 1149.1-compliant boundary scan cells	Automates process of adding comprehensive, standard boundary scan support for testing IC I/O cells and board-level interconnects between ICs.
1149.1 Custom Cell Boundary Scan	Automates support for full-custom boundary scan cells, including cell integration and verification Supports mixed use of full-custom and LogicVision boundary scan cells	All benefits of 1149.1 standard boundary scan while allowing the flexibility to use full-custom boundary scan cells, including those in third-party IP.
IEEE 1149.6 Boundary Scan	Generates and integrates RTL code for 1149.6-compliant TAP controller and boundary scan cells. Provides noise tolerance required for differential, AC-coupled nets.	All benefits of 1149.1 standard boundary scan while adding support for differential I/O cells driving AC-coupled nets. Full compatibility with 1149.1 scan.
1149.1-Based Contactless I/O Test	Tests for all I/O stuck-at, pull-up and tristate faults. Measure positive and negative leakage currents (IIL and IIH) without contacting bond pads on any tester.	Faster, reduced-pin-count testing at wafer-sort and final test. Higher yield through avoidance of contact resistance and loadboard leakage/noise.

PRODUCT DESCRIPTION: STANDARD 1149.1 SUPPORT

ET*Boundary* provides a completely automated solution for adding 1149.1 standard boundary scan support to ICs of any size or complexity. This standard enables fast, effective test of I/O cells and internal logic using low pin-count testers. This reduces test cost while improving IC yield.

1149.1 also supports test of board-level interconnects between ICs without requiring bed-of-nails board testers. This reduces board test cost while detecting interconnect problems before shipment to the field. ET*Boundary* automatically generates the RTL code for the TAP controller and boundary scan cells, and automatically integrates these into the design RTL. It also generates the scripts required for logic synthesis of the RTL, a BSDL description of the boundary scan functionality, simulation testbenches to verify the correctness of the boundary scan, and test patterns for manufacturing test of the IC.

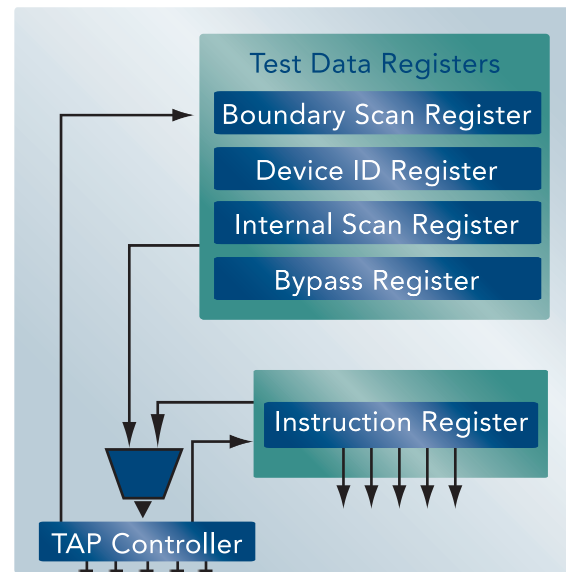
This completely eliminates the design phase for boundary scan logic and I/O cells, and automates the integration and verification of the boundary scan solution.

BENEFITS

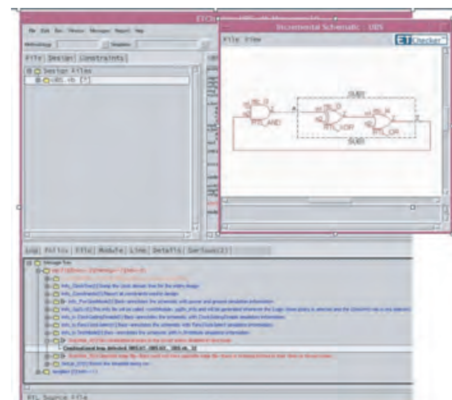
- Reduced Field Returns:
  - IC I/O cell problems detected before shipment
  - Inter-IC board problems detected before shipment
- Shortened Time-To-Market:
  - Quick boundary scan design-for-test (DFT) integration
  - Automated rule checking with interactive debug
  - IEEE 1149.1 standard support for quick integration into board test programs
- Reduced IC Development Costs:
  - Ready-to-use library of boundary scan cells
  - Testbenches to automate verification in simulation

CAPABILITIES

- Comprehensive testing for I/O cells, bonding, and board-level interconnects
- No capacity limitations for high-pin-count ICs
- TAP can be customized to include user-defined instructions and data registers
- Leverages any existing JTAG multiplexers in I/O cells
- Fully plug-and-play compatible with the complete set of LogicVision Embedded Test products and capabilities



IEEE 1149.1 Architecture



Rule Checking with Interactive Debug

PRODUCT DESCRIPTION: STANDARD 1149.1 CUSTOM CELL OPTION

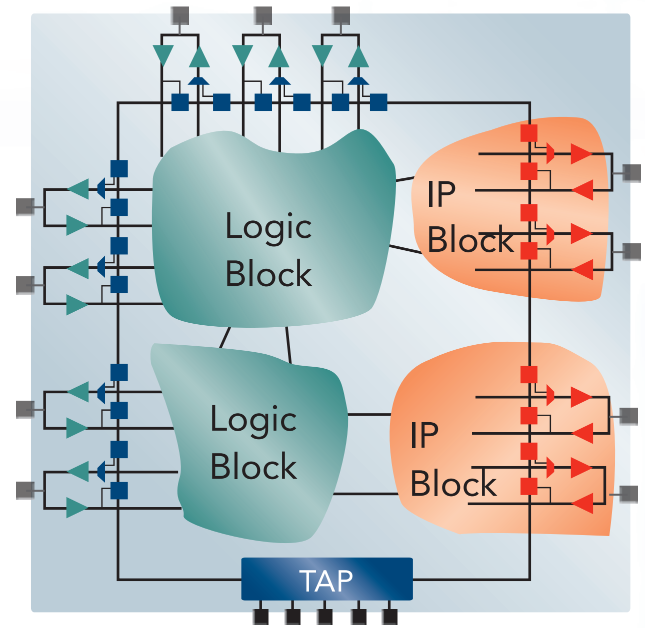
ET*Boundary* provides an option to support custom boundary scan cells, including those contained within third-party IP blocks. Custom boundary scan cells can be intermixed with ET*Boundary*–generated scan cells. This option supports custom cell integration and verification, and generates a BSDL description of the boundary scan functionality based upon a user-supplied library file describing the custom boundary cells.

BENEFITS

- Reduced Field Returns:
  - All the benefits of 1149.1 standard boundary scan
- Shortened Time-To-Market:
  - All the benefits of 1149.1 standard boundary scan
- Reduced IC Development Costs:
  - Simple library specification for custom scan cells
  - Testbenches to automate verification in simulation

CAPABILITIES

- All the capabilities of 1149.1 standard boundary scan
- Freely intermixed standard boundary scan cells, custom boundary scan cells, and boundary scan cells in IP blocks



Connection of Boundary Scan Cells Inside IP

PRODUCT DESCRIPTION: STANDARD 1149.6 OPTION

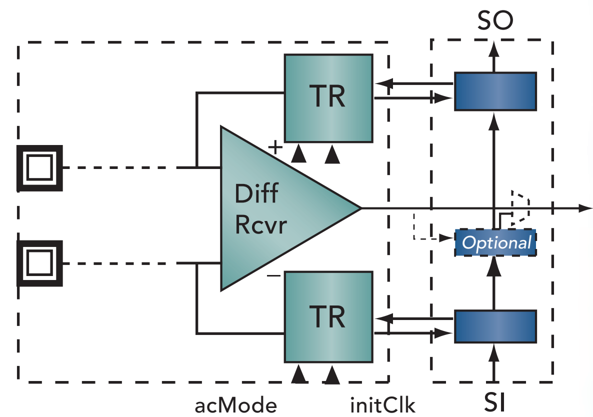
ET*Boundary* provides an option for applying 1149.6 boundary scan to differential, AC-coupled nets. The 1149.6 standard is required since 1149.1 assumes DC input levels, DC threshold voltages, and no noise. None of these characteristics is true for differential, AC-coupled nets. However, 1149.6 is completely compatible and compliant with 1149.1, so the same boundary scan solution can link together different types of I/O cells.

BENEFITS

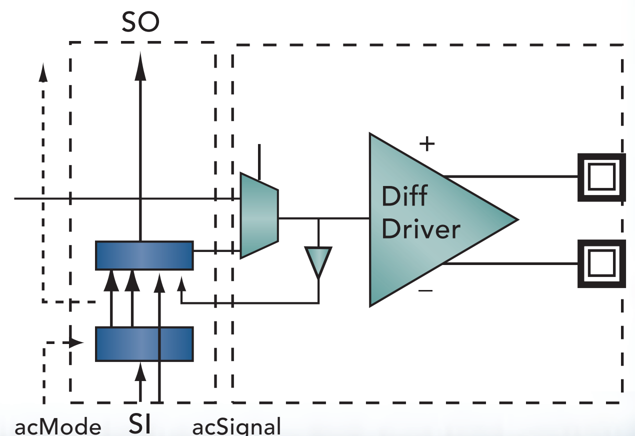
- Reduced Field Returns:
  - All the benefits of 1149.1 standard boundary scan
- Shortened Time-To-Market:
  - All the benefits of 1149.1 standard boundary scan
- Reduced IC Development Costs:
  - Automated generation, integration and verification of 1149.6 boundary scan
  - Example HDL code for receiver and driver pad models
  - Testbenches to automate verification in simulation

CAPABILITIES

- All the capabilities of 1149.1 standard boundary scan
- Automatic creation of 1149.6-compliant TAP controller
- Automatic creation and integration of 1149.6-compliant receiver and driver RTL boundary scan cells
- Tolerates up to 1/2 TCK skew in all signals
- Supports diagnostic capabilities, including contact-less pinleakage test



1149.6 Receiver Configuration



1149.6 Driver Configuration

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PRODUCT DESCRIPTION: 1149.1-BASED CONTACTLESS I/O TEST OPTION

Reduced-pin-count test, in which many signal pads are not probed, is commonly used for high-pin-count ICs. If the unprobed pads are bi-directional and boundary-scan accessible, then the path to and from each pad can be tested for stuck-at faults. Although DC parametric tests are typically performed, by far the most likely DC parametric test to fail is pin leakage current. Besides being an important pin specification, it is a sensitive indicator of the IC's reliability and process control.

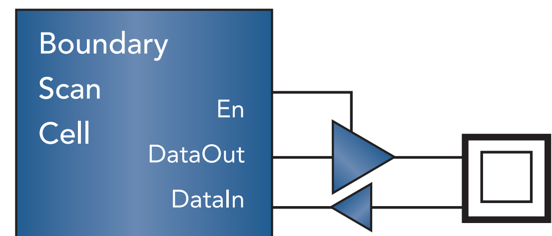
The ET*Boundary* contactless I/O option generates a fast test to structurally measure positive and negative leakage currents (IIL and IIH), and compare them to test limits. This process entails pre-charging each pad to a logic value, tri-stating the pad, and then capturing the pad's logic value a precise time later that is dependent on the pad's capacitance and the leakage current. If the current is excessive, the logic value will have changed. If the tri-state enable is stuck on, this test will always pass, so ET*Boundary* also generates a test to detect whether the pin can be tri-stated. Odd and even pins are tested separately to detect leakage between adjacent pins. ET*Boundary* also respects any constraints for simultaneously switching outputs (SSOs).

BENEFITS

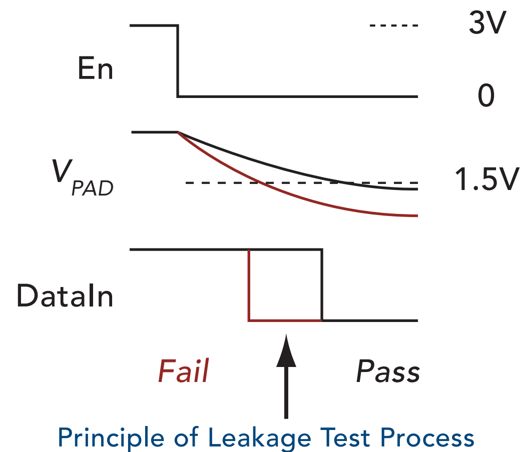
- Faster I/O test, without requiring a PMU, on any tester
- Fewer contact problems, producing higher overall yield
- Multi-site test of SoCs to reduce test cost
- Simpler, lower cost probe cards for high-pin-count ICs
- Improved board-level fault coverage

CAPABILITIES

- Test pin leakage, at wafer-sort, without contacting the pins
- 50~5000 nA range, with 10 nA typical resolution
- 5 ms to test all I/O pins for IIL, IIH, and pin-to-pin leakage
- Tests for all stuck-at, pull-up, and tri-state faults
- Diagnoses faults in global or local pad driver enables
- No changes to boundary scan or bi-directional pad cells
- Robust, synchronous, purely digital operation
- On-chip comparison to test limits



Typical Bi-Directional Pad Connections



Principle of Leakage Test Process

ABOUT LOGICVISION

LogicVision, Inc. (NASDAQ: LGVN), provides unique test and yield learning solutions in the design for manufacturing space. These capabilities enable its customers, leading semiconductor companies, to more quickly and efficiently learn to improve product yields. The company's advanced Design for Test (DFT) product line, ET*Create*™, works together with ET*Access*™ and Yield Insight yield learning applications to improve profit margins by reducing device field returns, reducing test costs, and accelerating both time to market and time to yield. LogicVision solutions are used in the development of semiconductor ICs for products ranging from digital consumer goods to wireless communications devices and satellite systems. LogicVision was founded in 1992 and is headquartered in San Jose, California. For more information visit www.logicvision.com.

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