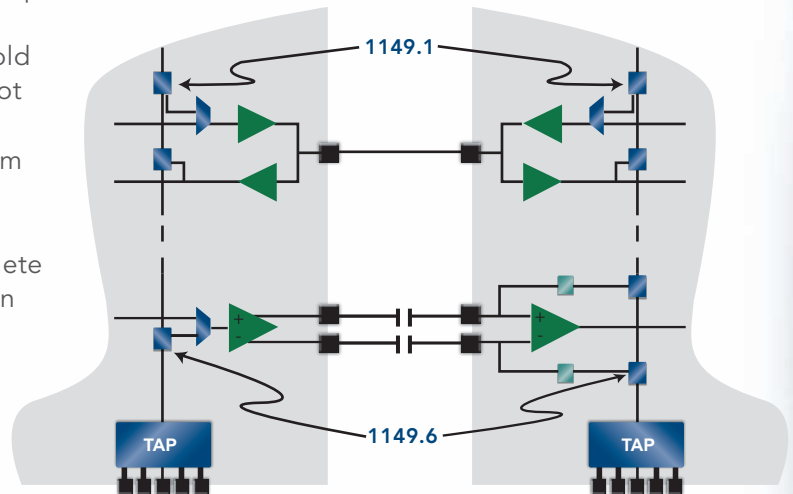




# ETBoundary™-1149.6

## OVERVIEW

The IEEE 1149.1 boundary scan standard was developed to test board-level interconnect nets between ICs. The standard assumes DC input levels, DC threshold voltages, and no noise. These characteristics do not apply to differential or AC-coupled nets. The IEEE 1149.6 standard was developed to address this form of interconnect required for increasingly popular differential I/O such as high-speed SerDes. LogicVision's ETBoundary-1149.6 provides a complete solution for the automated creation and integration of IEEE 1149.6 boundary scan cells and related control logic. This solution also supports, and is fully compatible and compliant with, the IEEE 1149.1 standard, allowing boundary scan cells from both standards to be placed on the same chip. Access to all boundary scan cells is provided through a common Test Access Port (TAP) interface that supports both standards.



Board-level Interconnect Test Solutions

## CAPABILITIES

- LogicVision's 1149.1 boundary scan automation
- Automatic creation of 1149.6-compliant TAP controller
- Automatic creation and integration of 1149.6-compliant receiver and driver RTL boundary scan cells
- Automatic creation of I/O manufacturing test patterns
- Tolerates up to 1/2 TCK period skew in all signals
- No capacity limitations for high-pin-count ICs
- TAP can be customized to include user-defined instructions and data registers
- Leverages any existing JTAG multiplexers in I/O cells
- Fully plug-and-play compatible with the complete set of LogicVision BIST products and capabilities

## BENEFITS

- Reduced Field Returns:
  - › IC I/O cell problems detected before shipment
  - › Inter-IC board problems detected before shipment
- Shortened Time-To-Market:
  - › Quick boundary scan design-for-test (DFT) integration
  - › Automated rule checking with interactive debug
  - › IEEE 1149.1 protocol support for quick integration into board test programs
- Reduced IC Development Costs:
  - › Ready-to-use library of boundary scan cells
  - › Example HDL model for I/O receiver and driver
  - › Testbenches to automate verification in simulation

## SUPPORTED BOUNDARY SCAN CELLS AND TIMING

The ETBoundary-1149.6 solution supports generation of boundary scan cells that match a wide range of different AC-pad types, including:

- Input-only, output-only, or bi-directional pads.
- Pads where the JTAG muxes are located inside the pad, inside the core, or inside the boundary scan cell.
- Single-ended or differential pads.

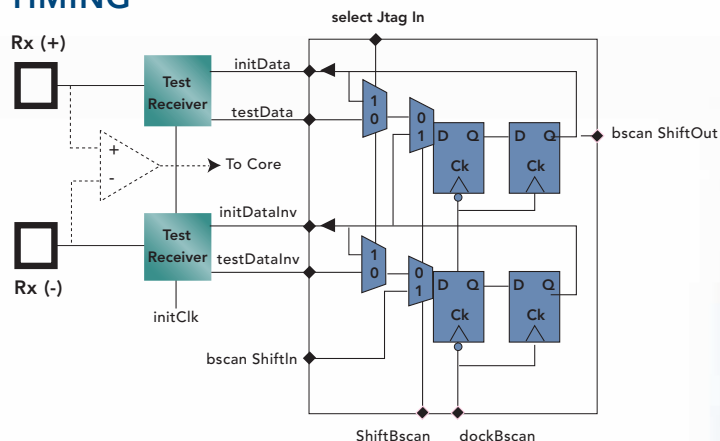
In addition, a number of options can be specified on a per boundary scan cell basis:

- Input or bi-directional boundary scan cells can either ignore, sample, or intercept the functional input signal going to the core.
- Output AC pads can be grouped to permit enabling of the AC test mode of only one group at a time.

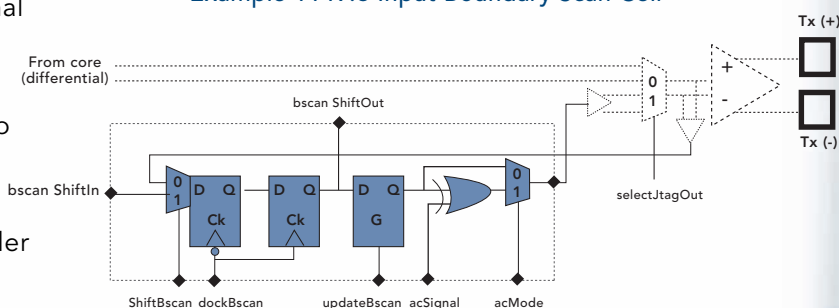
An enhanced TAP controller is also generated and linked to all boundary scan cells. The controller sources the three mandatory IEEE 1149.6 control signals:

- **acMode**—indicates that either the EXTEST\_PULSE or EXTEST\_TRAIN instruction is active.
- **acSignal**—carries the output state inversion signal used by all IEEE 1149.6 output boundary scan cells.
- **initClk**—the initialization signal used by all AC input pads.

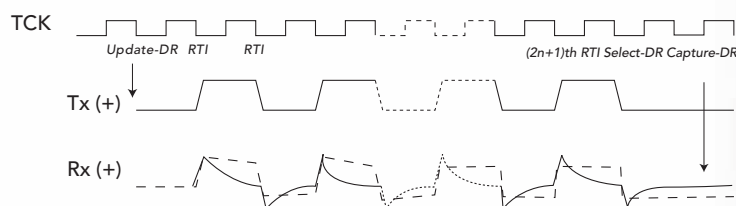
These signals generate all of the required IEEE 1149.6 timing waveforms.



Example 1149.6 Input Boundary Scan Cell



Example 1149.6 Output Boundary Scan Cell



1149.6 Timing Waveforms (EXTEST\_TRAIN mode)

## ABOUT LOGICVISION

LogicVision (NASDAQ: LGVN) provides proprietary technologies for embedded test and yield learning that enable more efficient manufacturing test of complex semiconductors. LogicVision's embedded test solutions allow integrated circuit designers to embed test functionality into a semiconductor design that is used during semiconductor production test and throughout the useful life of the chip. The company's advanced

Design for Test (DFT) product line, ETCreat™, works together with Silicon Insight™ and Yield Insight™ applications to improve profit margins by reducing device field returns and test costs, accelerating silicon bring-up times and shortening both time to market and time to yield. For more information on the company and its products, please visit the LogicVision website at [www.logicvision.com](http://www.logicvision.com).

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